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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/637,016	08/14/2000	Peter Ka-Fai Chow	95-332	8308
20736	7590	02/09/2004	EXAMINER	
MANELLI DENISON & SELTER 2000 M STREET NW SUITE 700 WASHINGTON, DC 20036-3307			MOORE, IAN N	
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			2661	6

DATE MAILED: 02/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/637,016

Applicant(s)

CHOW ET AL.

Examiner

Ian N Moore

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, and 8 is/are rejected.
- 7) ☒ Claim(s) 3-7 and 9-14 is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed January 16, 2004 have been fully considered but they are not persuasive.

In response to applicant's argument that Harriman'687 is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Harriman'687 is the packet/cell switch, which is the analogue art to applicant invention (see Harriman'687 col. 1, line 5-7).

Regarding claims 1,2, and 8, the applicant alleged, "Harriman's prior art switch is not within the field of the inventors' endeavor, namely providing layer 2 and above switching of data packets in a non-blocking network switch configured for switching data packets between subnetworks."

In response applicant's argument, claim 1 broadly recites, "...receiving, at a network switch port, at least a portion of a data frame **including layer 3 information...**" Claim 1 recites neither "a layer 3 switch", "a layer 2 and above switch", "a switching/switch only performs in layer 3", nor "a switching/switch only performs in layer 2 and above". Thus, it is noted that the features upon which applicant relies (i.e., layer 3, or layer 2 and above) are not recited in the rejected claim(s). Although the claims are interpreted in light of

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the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

The applicant alleged, regarding claim 1 and 8, “Harriman provides no disclosure or suggestion of using a switch fabric configured for receiving a tag result and for performing a frame forwarding decision based on the tag result”.

In response applicant’s argument, claim 1 does not recite, “...receiving a tag result and for performing a frame forwarding decision based on the tag result...” In addition, examiner asserts, receiving a tag result as a new header and assembler 116 performing the forwarding to packets based upon the new header. Also, it is well known in the art that the routing tag/tags must be present in the header in order to identify where to route. Thus, a tag result is a new header.

The applicant alleged, “Harriman does not teach generating a tag result outside of the switch fabric 110”.

In response to applicant's argument, examiner acknowledges that a typographical error in the “reference label” was made in claim 8 rejection as “Assembler 110” (page 6, line 1), instead of “Assembler 116”; however, it is obvious to one skill in the ordinary art that the assembler is performing the function of the switching by receiving the OTF and forwarding/switching to the output port. Examiner asserts **assembler 116** as a switch fabric and OTF 112 as a tag result.

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The applicant alleged, in claim 8, "Harriman does not disclose a switch port having port filter to generate a tag result.... The port 102 of Harriman does not generate a tag result." ✓

In response to applicant's argument, examiner asserts that the port filter as combined system of extractor 114, ITF 120 and/or OTF 122 (see Harriman'687 FIG. 1) since the combined system performs identical function/operation as a port filter, that is, generating a new header (i.e. a tag result).

In view of the above, examiner believes that the reference as set forth in the 103 rejections is proper, thus, Claims 1, 2 and 8 are obvious over Harriman'687 in view of well established teaching in the art for at least the reasons discussed above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claim 1,2, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harriman (U.S. Patent 5,898,687) in view of well establishing teaching of the art.

Regarding claim 1, Harriman '687 discloses a method of synchronizing transfer of frame tags to a switch fabric with the transfer of data frames to a buffer memory, the method comprising:

receiving, at a network switch port (Input ports 102; see Fig. 1), at least a portion of a data frame including layer 3 information (a conventional extraction circuit 114 that apportions each cell received at the switching fabric 110 into its constituent payload and header information fields; see col. 4, line 7-11. Also, upon receiving a cell, the switching fabric extracts the payload data from the cell, stores it in the shared memory and records the memory address of that payload location in an address pointer; see col. 2, line 16-19. Noted that when a frame is received with a header, it must contain source and destination addresses (i.e. Layer 3) in order to translate or tagging the header),

generating a tag result corresponding to at least a portion of the data frame (an output translation function (OTF) 122 connected to the assemble circuit 116. As described herein, these translators cooperate to convert the contents of each received cell header field to a new header in connection with conventional translation methods; see col. 4, line 14-19. Noted that a tag result (i.e. new header) is generated at least a portion of a frame); and

synchronizing transfer of the tag result to a switch fabric (Assembler 110; Fig.1) with a transfer of at least a portion of the data frame to a buffer memory (Share Memory 112; Fig.1) based on a signal (output line 255 of the selector 252; see Fig. 1 and Fig.2) indicating a status of the transfer of the portion of the tag result to the switch fabric (referring to FIG. 1, the selected pointer address on line 255 is fed to the shared memory unit 112 in order to retrieve the corresponding cell payload information over line 118. The assemble circuit 116

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of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. OTF 122 derives this header information in response to the connection address generated by the ITF 120. The header information is preferably stored in an output header table (not shown) of the ITF 120; see col. 7, line 56-64).

Harriman '687 does not explicitly disclose sending a signal from the buffer memory in order to synchronize.

This limitation is obvious and well known in the art. Noted that Harriman '687 discloses sending a notifiicator/pointor (i.e. transfer indication signal) via an output line to the share data memory buffer regarding the transfer indication of a new header (i.e. tag results) in order to synchronize at the assembler (i.e. Switch fabric). The goal of synchronizing is to avoid incorrect tagging or mis-assembling between new header and the payload data. Furthermore, Harriman '687 teaches sending a notification/pointing/signal initially to the payload data buffer memory by instructing where to begin, where the payload should be, and where the new header will be at the assembler before combining the header and the payload data. Also noted that it is also possible to send a notification/pointer/signal initially from the payload data buffer memory in order to achieve the same goal of synchronizing.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Harriman '687 as taught by well known established teaching for the purpose of synchronizing the tagging process between the data and the tag/header at the switch. The motivation being that by implementing the

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synchronization mechanism, it can avoid the delay of header processing and misordering/mistagging the payload data.

Regarding claim 2, Harriman '687 discloses storing the portion of the data frame in the buffer memory (see Harriman '687 see col. 8, line 31-32; extracting the data portion from the data element and storing that portion in a location of memory).

Regarding claim 8, Harriman '687 discloses a network switch comprising:

a switch port (Input Port 102; Fig. 1) having a port filter (a combination of Extractor unit 114 and Input Translation Function unit 120 (ITF); Fig. 1) configured to receive at least a portion of a data frame including layer 3 information and to generate a tag result (a conventional extraction circuit 114 that apportions each cell received at the switching fabric 110 into its constituent payload and header information fields; see col. 4, line 7-11. Also, upon receiving a cell, the switching fabric extracts the payload data from the cell, stores it in the shared memory and records the memory address of that payload location in an address pointer; see col. 2, line 16-19. Noted that when a frame is received with a header, it must contain source and destination addresses (i.e. Layer 3) in order to translate or tag the header),

a queue block (Share memory 112; Fig. 1) configured for transferring the data frame from the switch port to a buffer memory (extracting the data portion from the data element and storing that portion in a location of memory; see col. 8, line 31-32),

a switch fabric (Assembler 116; Fig. 1) configured for receiving the tag result and for performing a frame forwarding switching decision based on the tag result (i.e. new header)

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and monitoring of the transfer of the data frame (an output translation function (OTF) 122 connected to the assemble circuit 116. As described herein, these translators cooperate to convert the contents of each received cell header field to a new header in connection with conventional translation methods; see col. 4, line 14-19. Moreover, the assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. OTF 122 derives this header information in response to the connection address generated by the ITF 120; see col. 7, line 59-65. Noted that assembler unit is responsible for forwarding the frame according to the new address/tag in the new header by communicating with OTF unit).

a synchronizing device (Output Translation Function 122 (OTF); Fig.1) configured to synchronize the transfer of the tag result to the switch fabric with the transfer of the at least a portion of the data frame to the buffer memory based on a signal (output line 255 of the selector 252; see Fig. 1 and Fig.2) indicating a status of the transfer of the portion of the tag result to the switch fabric (referring to FIG. 1, the selected pointer address on line 255 is fed to the shared memory unit 112 in order to retrieve the corresponding cell payload information over line 118. The assemble circuit 116 of switching fabric 110 appends new header information on line 124 to the payload data retrieved on line 118 prior to transmitting the selected cell of the output cycle. This header information is derived by OTF 122 in response to the connection address generated by the ITF 120. The header information is preferably stored in an output header table (not shown) of the ITF 120; see col. 7, line 56-64).

Harriman '687 does not explicitly disclose a synchronizing device (Output Translation Function 122 (OTF); Fig.1) sending a signal (i.e. output line that notify the share

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memory buffer the location of payload to be added and transmitted along with a new header) to the buffer memory.

This limitation is obvious and well known in the art. Noted that Harriman '687 discloses OTF sending a notifiicator/pointor (i.e. transfer indication signal) via an output line to the share data memory buffer regarding the transfer indication of a new header (i.e. tag results) in order to synchronize at the assembler (i.e. Switch fabric). The goal of synchronizing is to avoid incorrect tagging or misassembling between new header and the payload data. Furthermore, Harriman '687 teaches sending a notification/pointing/signal initially to the payload data buffer memory by instructing where to begin, where the payload should be, and where the new header will be at the assembler before combining the header and the payload data. Also noted that it is also possible for the data buffer to initially send a notification/pointer/signal to the OTF (i.e. synchronization device) regarding the transfer indication in order to achieve the same goal of synchronizing.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Harriman '687 as taught by well known established teaching for the purpose of synchronizing the tagging process between the data and the tag/header at the switch. The motivation being that by implementing the synchronization mechanism, it can avoid the delay of header processing and misordering /mistagging the payload data.

Allowable Subject Matter

2. Claim 3-7, 9-13, and amended claim 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 703-605-1531. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 703-308-7828. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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KENNETH VANDERPUYE
PRIMARY EXAMINER